REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 1-2, 4-9, 15, and 22-23 are now pending, with claim 1 being independent.

Claim 1 has been amended to include the limitation from dependent claim 2 of the flat outline substantially parallel to the chip surface.

As amended, claim 1 presents a semiconductor device that includes a semiconductor chip with a planar active surface. The planar active surface has an integrated circuit protected by an inorganic overcoat, the integrated circuit having metallization patterns with a plurality of contact pads. As shown in Figure 2, each of the contact pads 202 has an added conductive layer 205 on the metallization patterns. The added conductive layer 205 has a conformal surface adjacent the semiconductor chip that includes peripheral portions 205a of the inorganic overcoat 203. The added conductive layer 205 also has a planar outer surface 206, 207 defining a flat outline substantially parallel to the chip surface (surface of inorganic overcoat 203), the planar outer surface suitable to form metallurgical bonds without melting.

Independent claim 1 stands rejected under 35 U.S.C. § 102(e) as obvious over Lin et al. (6,426,556). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Lin does not describe or suggest that the added conductive layer has a planar outer surface defining a flat outline substantially parallel to the chip surface.

Lin, in relevant part, describes a method for creation of metal bumps over surfaces of I/O pads by depositing and etching layers of material. As shown in Figure 9, a substrate 10 has a dielectric layer 29 deposited on top of the substrate. Figure 9 shows an aluminum contact pad 24 over the layer of dielectric 29 with a probe mark 28 on surface of contact pad 24 caused by repetitive contacting by a tester probe. Next, a passivation layer 32 is deposited over the surface of layer 29 of dielectric and an opening created in the layer of passivation 32 that aligns with aluminum contact pad 24. Figure 11 shows a cross section of the substrate 10 after the contact pad 24 has been etched to create opening 36. Figure 12 shows a cross section after layer 33 of under bump metal (UBM) has been created over the surface of contact pad 24. Figure 13 shows a layer 39 of photoresist deposited over layer 33 of UBM. Layer 39 of photoresist is patterned

and developed, creating an opening 38 in the layer 39 of photoresist. Next, a layer 34 of enhanced UBM is electroplated over the layer 33 of UBM. Next, as shown in Figure 14, the layer 35 of bump metal is electroplated in contact with the layer 34 of enhanced UBM. Figure 15 shows a cross section after the layer 39 of photoresist has been removed. UBM layer 33 is etched using bump metal 35 as a mask. As shown in Figure 15, the chip surface on passivation layer 32 includes a ridge. Thus, Lin does not describe or suggest that the added conductive layer has a planar outer surface defining a flat outline substantially parallel to the chip surface but rather a planar outer surface of a conductive layer having a flat outline perpendicular to the chip surface at the ridge. As shown in Applicant's Figure 2, the planar outer surface of the added conductive layer defines a flat outline that covers the ridges on the chip surface. In Lin, metal layer 35, enhanced UBM layer 34, and UBM layer 33 shown in Figure 15 would have to extend in both directions to cover the ridge generated by passivation layer 32 and create a flat outline substantially parallel to the chip surface.

The planar outer surface of the added conductive layer defining a flat outline substantially parallel to the chip surface provides several advantages. In particular, the flat outline of the planar outer surface substantially parallel to the chip surface and covering ridges around the contact pad reduces stress and cracking along the chip surface and along the bond with the terminal pads of the wiring board, resulting in improved reliability of the device.

For at least the reasons given above, Applicants respectfully submit that claim 1 is patentable over Lin.

Claims 2, 4-9, 15, and 22-23 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 2, 4-9, 15, and 22-23 for at least the reasons discussed above with respect to claim 1.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,556) in view of Kleffner et al. (5,943,597). However, Kleffner fails to remedy the failure of Lin to describe or suggest that the added conductive layer has a planar outer surface defining a flat outline substantially parallel to the chip surface. Kleffner describes use of a trench for stress relief in a bumped semiconductor device as shown in Figure 2. The bumped semiconductor device includes a bond pad 12 formed on a semiconductor die 10. A solder bump 22 is formed so as to overlie the bond pad 12 through a UBM conductive layer 18. A stress isolation trench

15 is formed in a passivation layer 14, so as to surround the solder bump 22. Kleffner does not describe or suggest that the conductive layer 18 has a planar outer surface defining a flat outline substantially parallel to the chip surface but rather a curved surface because of the solder bump 22. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,556) in view of Elenius et al. (6,287,893). However, Elenius fails to remedy the failure of Lin to describe or suggest that the added conductive layer has a planar outer surface defining a flat outline substantially parallel to the chip surface. Elenius describes, as shown in Figure 2, a chip scale package 8 for a flip chip integrated circuit 10 that includes a redistribution conductive layer 30 upon the upper surface of a semiconductor wafer 14 for simultaneously attaching to solder balls 28 as well as with the conductive bond pad 18 of the underlying integrated circuit. Elenius does not describe or suggest that the conductive layer 30 has a planar outer surface defining a flat outline substantially parallel to the chip surface but rather an outer surface interrupted by a large sphere-like solder ball as shown in Figures 2 and 3 for attachment to a circuit board. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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